design FAQs Direct Digital Synthesis

FREQUENTLY ASKED QUESTIONS

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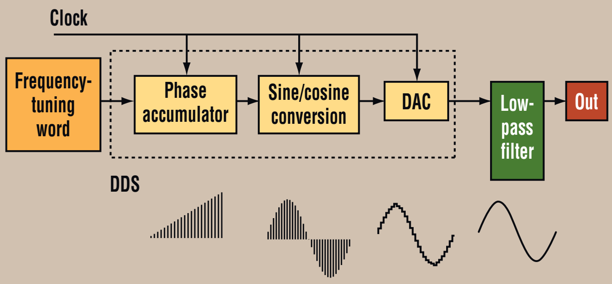

These are the basic functions of direct digital synthesis, with representative waveforms.

How does direct digital synthesis (DDS) work?

There are at least three elements to DDS: a numerically controlled oscillator (NCO) with a phase modulator, a block that converts the phase information to amplitude values, and a digital-to-analog converter (DAC). An in-phase/quadrature (I and Q) modulator may be added ahead of the DAC.

Here's the theory. In a sinusoidal wave in the analog domain, the phase angle of a single frequency, f_a, rotates though a fixed angle at a rate of:

$$\omega \text{ (or } \Delta\text{phase}/\Delta t) = 2\pi f$$

That angular rate of change with respect to time is a linear ramp proportional to the sine wave frequency that returns to zero at the end of each sine wave cycle. In the digital domain, Δt in the expression above becomes the reciprocal of the sample-clock frequency, f_s. This implies that, for any given sample:

$$f_a = (\Delta\text{phase} * f_s)/2\pi$$

The phase accumulator in the DDS assembles the phase component of the output signal, typically based on a 32-bit frequency-tuning word (FTW) that represents the desired value of Δphase. Clearly, 32 bits provide very fine resolution of the DDS's output frequency. To accomplish phase modulation, a phase offset can be added by means of a separate phase register.

This phase information maps directly into a sequence of amplitude values for the frequency specified by the input word. A block in the DDS then converts that phase information into amplitude values.

Traditionally, sine/cosine lookup tables in memory have accomplished this task. To keep the size of the lookup table manageable, not all of the bits in the FTW are used in the lookup, although they do provide fine resolution in selecting f_a. The output of this block is the input to the DAC, which generates a sequence of amplitudes. A low-pass filter smoothes the output of the DAC.

What are the advantages of DDS?

The digital nature of DDS technology provides flexibility, repeatability, and precision. The output is digitally calculated, so it does not deviate over time as long as the reference clock is stable. With careful attention to frequency planning, it also can enhance spurious-free dynamic range (SFDR).

What kinds of applications employ DDS?

Originally, DDS was used to provide tunable local oscillators and signal generators and to implement various modulation schemes. The latest DDS chips are used in those functions as well as in medical imaging, single-sideband suppressed-carrier modulation, phased-array radar and sonar applications, clocking, and acousto-optic tunable filters (AOTFs).

An AOTF is a solid-state electronically tunable spectral-bandpass filter. AOTFs make it possible to extract a single wavelength from multiline or broadband light sources. An RF frequency applied to the AOTF transducer controls the output-light wavelength, while the RF amplitude controls the light's intensity.

What's the history of monolithic DDS chips?

Although DDS technology has been in use since at least the 1970s, it was implemented using separate chips until the mid-1990s. The slowest and most expensive element, the DAC, limited its performance. The first monolithic DDS chips appeared in 1994. They integrated the DAC on the same substrate as the other circuit elements, simplifying implementation and lowering costs.

What's different about the latest DDS chips?

Two- and four-channel chips with guaranteed 72-dB channel-to-channel isolation for two channels and 65 dB for the quad chip are available. They operate from clocks as fast as 500 Msamples/s, producing output frequencies from dc up to 200 MHz in 116-mHz steps. (F_{MAX} is slightly below the Nyquist criterion because harmonics mixed with the clock show up in-band and are too close to be filtered.)

Architecturally, algorithms are replacing lookup tables, providing a more efficient method of converting phase data to amplitudes. A new feature allows synchronous loading of updated amplitude, frequency, and phase information for all channels. The updates take place simultaneously.

Performance-wise, SFDR is higher. The FTW updates more quickly, too. In the fastest new ICs, it updates in 50 ns, which is 32 times faster than in previous chips. For all that, power consumption is lower, down around 165 mW per channel in multichannel DDS chips.

Parts can be programmed for any combination of two-level direct modulation, linear sweep, or single-tone generation without pin constraints. Within certain limits, the simultaneous operation of four-, eight-, and 16-level modulation is possible.

Alternatively, amplitude, frequency, or phase can be modulated. Frequency ramp-up and ramp-down make it possible to increase or decrease the amplitude before and after the modulated data sequence. Linear sweep provides precision stepping of amplitude, frequency, or phase between two points.

What else is new about the latest DDS chips?

Before the advent of multichannel DDS chips, the external delay between ICs made synchronization difficult. Some new dual-channel and quad-channel chips let designers select phase offsets relative to each channel. Improved synchronization techniques can manage applications with more channels.

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