POWER

DESIGN FAQs

Frequently Asked Questions:

NEW INDUSTRIAL ANALOG PROCESS TECHNOLOGIES

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In the early days of analog ICs, chip designers had a large arsenal of circuit elements that let them create products with exceptionally high performance. Over time, to keep analog IC prices competitive, analog process technologies followed the lead of digital CMOS. Analog chip designers then found themselves with fewer and fewer magic analog bullets they could use to design new products. This has been particularly hard on engineers who design "industrial" mixed-signal systems, because they now find themselves squeezed between the relatively high-voltage world of their sensors and actuators and the ever diminishing operating and threshold voltages of successive CMOS generations.

In a welcome countertrend, analog/mixed-signal IC companies are developing new process technologies that permit mixing voltages on a single die as well as combinations of CMOS, high-voltage MOS, and high- and low-voltage bipolars. As a result, analog chip designers are again expanding their arsenals. Competition will continue to encourage innovation and improve performance.

What, exactly, are "industrial" analog and mixed-signal applications?

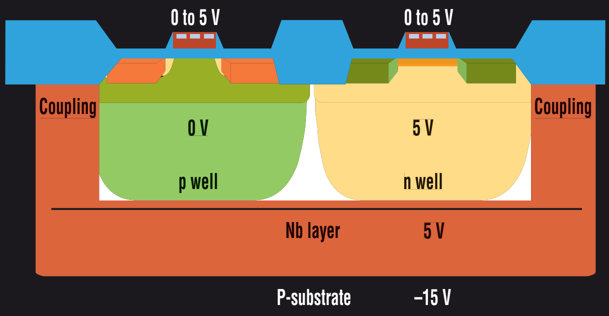
Generally, the term encompasses factory automation and process control, instrumentation (both automatic test equipment and bench gear), medical products (ranging from MRI and CAT-scan equipment to portable diagnostic instruments and personal testers for glucose and fever temperature), and automotive (airbags, ABS, ignition control, active suspension, and tire-pressure monitoring). Taken together, these applications represent more than 30% of the market for data converters and signal-conditioning electronics.

What's the problem with using advanced CMOS-based analog chips in industrial designs?

Engineers who create these systems are squeezed between the relatively high, often differential voltages at which their sensors and actuators operate and the voltage limits of the latest CMOS. Consequently, they've had to add more and more signal conditioning built on older technologies on either side of their converters and control systems. This approach is expensive and power-hungry, and it wastes board space.

What does a multidevice technology provide to analog chip designers?

A multidevice technology makes it possible to isolate components from the substrate and from each other so a single chip can mix and match 5-V CMOS with higher-voltage 16-, 24-, or 30-V CMOS and bipolar devices, with multiple voltage supplies running to the same chip. Amplifiers for signal conditioning benefit from the availability of bipolar because it's possible to match devices. They also provide the largest possible gm for any given power consumption. The availability of MOS devices makes it possible to achieve switched-capacitor filters that can accommodate high input voltages. And of course, digital post-conversion signal processing can take place on the same die using fine-line CMOS.



With a multidevice technology, both 5-V and high-voltage circuit elements can be fully isolated from the substrate and from each other. Isolation makes possible multiple voltage supplies to a single chip. For example, a ±15-V product with −15-V substrate bias also could include standard 5-V digital logic in a mixed-signal device.

Why hasn't something like this been done before now?

It takes a considerable level of commitment to overcome the conflicting demands of the different kinds of devices. Standard CMOS fine-line, low-voltage devices for the digital parts of the chips imply shallow junctions and thin oxides, low power consumption, and a small area. On the other hand, high-voltage devices require larger dimensions, deeper junctions, and thicker oxides, the processing of which degrades the performance of fine-line devices. Once designers have implanted shallow junctions and thin oxides, any subsequent processing on the die likely will cause those junctions to diffuse further, spreading them out and degrading their performance. Overcoming that conflict requires investing a lot of time and engineering to structure the process order of the different steps to control the thermal budget.

What about isolation?

If the analog portion of the die is going to use high-voltage bipolar supplies while the digital logic uses single-ended 5 V, isolation is going to be a major challenge. It all comes down to the silicon substrate's underlying voltage. If it's 0 V, isolating all the devices associated with a negative supply will be difficult. The number of necessary tubs and junctions also complicates process development and circuit design and layout. Instead, designers can connect the substrate to the most negative voltage in the system, which prevents unexpected biasing and the risk of latchup (see the figure). But this also makes it necessary to isolate the low-voltage CMOS in its own tub to eliminate back-gate effects from the negative voltage on the substrate.

Is a multidevice technology process manufacturable?

Yes. Creating junction isolation underneath the devices—deep wells for the low-voltage devices—provides vertical isolation while multiple guard rings and some deep diffusion to get down to the wells beneath provide horizontal. This requires more mask steps than plain vanilla CMOS. Fortunately, no one particular IC design needs to use all of the different mask sets. Yet it's a real challenge to develop all the possibilities and ensure they will work together regardless of which method any one circuit uses. It's also tricky to ensure the additional mask steps do not significantly reduce yield.

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