

TRUE CIRCUITS INC.™ | *timing is everything*

PRODUCT Q&As

TRUE CIRCUITS STANDARDIZED PLL AND DLL HARD MACROS

True Circuits, Inc. offers a complete family of award-winning, standardized PLL and DLL hard macros that spans nearly all performance points and features typically requested by ASIC, FPGA, and SoC designers.

All TCI PLLs feature our LockNow!™ Technology to dramatically improve PLL lock times. This is a significant advantage for chips that need fast restarts from low-power modes.

TCI DLLs delay a set of signals by precise and adjustable fractions of a reference clock cycle independent of voltage and temperature. They have flexible form factors and are ideal for high-speed DDR interface applications.

These PLLs and DLLs are available for immediate delivery in a range of frequencies, multiplication factors, sizes, and functions in TSMC, UMC, and Chartered processes from 0.25 μm to 90 nm.

Product Features

- Clock generator, low bandwidth, spread spectrum, and deskew PLLs
- DLLs for high-speed DDR and other interface applications
- Low-jitter and very process tolerant
- Versatile, with wide output frequency and multiplication ranges (1-4096)
- Small sizes and flexible form factors for easier integration
- TSMC, UMC, and Chartered processes from 0.25 μm to 90 nm

So what are you waiting for? Lock in a premium-quality, low-jitter PLL or DLL that you can count on for first silicon success. Go with True Circuits, the timing experts.

www.truecircuits.com/timing

4962 El Camino Real, Suite 206
Los Altos, CA 94022
650.691.2500
e-mail: timing@truecircuits.com

DESIGN FAQs

Frequently Asked Questions:

EVALUATING TIMING IP

Don Tuite, Analog/Power Editor

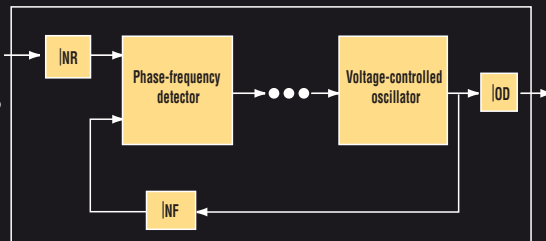
A phase-locked loop (PLL) is pretty basic. How much can one IP vendor's PLL differ from another's?

While the high-level PLL schematic is simple, the simplest PLLs don't perform well. They all accept a reference clock and generate another clock, frequency multiplied and/or phase-locked to the reference. Yet PLLs from different IP vendors offer different features, flexibility, and output quality. The right PLL can make the design of the clocking system easier and more robust by providing flexible clock multiplication capability and multiple phase-locked outputs at different frequencies or at different precise fractional phase offsets of the clock period. The wrong PLL can impede chip bring-up and production ramp by requiring lab work to discover process-dependent tweaking factors necessary to make the PLL operate as specified. There are differences in how closely vendors work with their licensees as well.

Are there objective criteria for PLLs?

Jitter and skew. The PLL has to work in a noisy mixed-signal environment, which leads to clock jitter. Jitter squeezes the time available to combinational logic, so lower jitter can help get your chip to timing closure faster. Skew, as well as jitter, can subtract from the timing margin between the chip

A basic PLL is deceptively simple: a divider on the reference clock input, a phase detector, a voltage-controlled oscillator, an output divider, and a divider on the feedback signal to the phase detector. From that starting point come frequency-spreading, de-skewing, and multiphase clocks.



with the IP PLL and the rest of the system. Dealing with them can make the system-design job harder, stretch development time, force the use of more expensive packaging, or even bomb the whole system design program.

How do I know how much clock jitter and skew I have to deal with on my custom chip?

Both on-chip jitter and on-chip static phase offset are difficult and expensive to measure accurately. That's why you need a good relationship with your PLL IP vendor—and a high level of trust. During design and after delivery of prototype and production silicon, the vendor can help chip designers characterize the clocking system of the IC in a way that expedites total system design. This also can help resolve interoperability issues that come up during system bring-up.

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