DESIGN FAQs

Frequently Asked Questions:

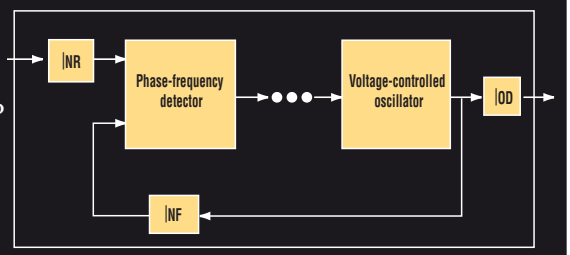
EVALUATING TIMING IP

Don Tuite, Analog/Power Editor

A phase-locked loop (PLL) is pretty basic. How much can one IP vendor's PLL differ from another's?

While the high-level PLL schematic is simple, the simplest PLLs don't perform well. They all accept a reference clock and generate another clock, frequency multiplied and/or phase-locked to the reference. Yet PLLs from different IP vendors offer different features, flexibility, and output quality. The right PLL can make the design of the clocking system easier and more robust by providing flexible clock multiplication capability and multiple phase-locked outputs at different frequencies or at different precise fractional phase offsets of the clock period. The wrong PLL can impede chip bring-up and production ramp by requiring lab work to discover process-dependent tweaking factors necessary to make the PLL operate as specified. There are differences in how closely vendors work with their licensees as well.

A basic PLL is deceptively simple: a divider on the reference clock input, a phase detector, a voltage-controlled oscillator, an output divider, and a divider on the feedback signal to the phase detector. From that starting point come frequency-spreading, de-skewing, and multiphase clocks.



Are there objective criteria for PLLs?

Jitter and skew. The PLL has to work in a noisy mixed-signal environment, which leads to clock jitter. Jitter squeezes the time available to combinational logic, so lower jitter can help get your chip to timing closure faster. Skew, as well as jitter, can subtract from the timing margin between the chip with the IP PLL and the rest of the system. Dealing with them can make the system-design job harder, stretch development time, force the use of more expensive packaging, or even bomb the whole system design program.

How do I know how much clock jitter and skew I have to deal with on my custom chip?

Both on-chip jitter and on-chip static phase offset are difficult and expensive to measure accurately. That's why you need a good relationship with your PLL IP vendor—and a high level of trust. During design and after delivery of prototype and production silicon, the vendor can help chip designers characterize the clocking system of the IC in a way that expedites total system design. This also can help resolve interoperability issues that come up during system bring-up.

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