design FAQs

Reducing FPGA Power Consumption

FREQUENTLY ASKED QUESTIONS

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Why do FPGAs consume so much power?

Historically, FPGAs have had a more passive "glue logic" role hardly worth mentioning in the overall power budget. But now they have taken over most of the system control, and today's FPGAs can be a system-on-a-chip (SoC) solution. That means they also consume a greater percentage of the total system power budget. But you can do several things at the chip and system levels to help meet your power budget.

What are the latest silicon innovations that help reduce power consumption?

As we move into deep-submicron geometries, increases in functionality per square millimeter come at the cost of higher static power consumption due to higher transistor leakage. Supplying the FPGA core voltage at the lower limit of the manufacturer's specification can save significant static power. For example, static power might increase 15% for a mere 5% increase in core voltage *(see the figure)*.

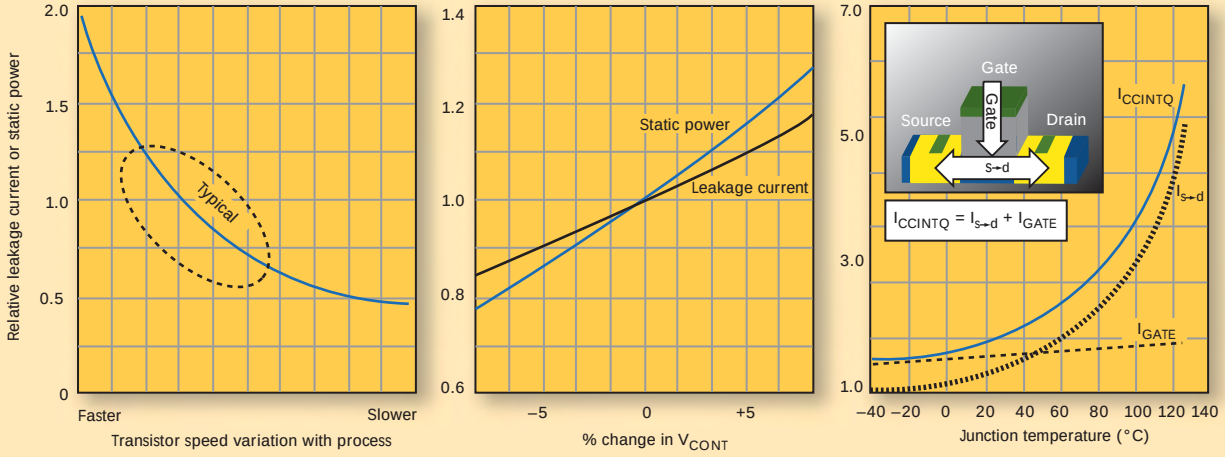
Some FPGA vendors use a triple-oxide process technology for some transistors to reduce static power consumption of non-speed-critical configuration circuitry. Another innovation is a shift to a coarser-grained logic architectures employing lookup tables (LUTs) with six inputs rather than the previous standard of four. This enables tighter logic packing, reduces the number of switching transistors, and shortens routing lengths, reducing dynamic power consumption.

How can power consumption be reduced at the chip level?

One of the more powerful techniques is to maximize the use of hard IP blocks available on chip, because FPGA vendors design the hard IP to use only the exact resources required to achieve a given protocol or architecture.

Another technique is to simply suspend all or part of the FPGA when it's not in use. Putting the FPGA "to sleep" when it's not in use is well understood. But even when it is in use, its ability to "shut off" parts that aren't needed for a given function often is overlooked. Internal RAM should be disabled when it's not in use. Use gated and/or local clocking to minimize power dissipation in the clock networks.

Also, take care when writing HDL code. Implement techniques like one-hot encoding for state machines and guarded evaluation while making sure you don't inadvertently create logic loops that oscillate. And finally, choose your I/O standards wisely, as



Small increases in core voltages can lead to large increases in static power. Conversely, a low core voltage can lower dynamic power consumption. (courtesy of Xilinx)

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some consume more static power than others.

How can tools help reduce FPGA power consumption?

One common mistake is to over-constrain FPGA timing or provide no timing constraints (whereby the tools may assume to try and build the fastest implementation possible). This leads the synthesis and place & route (P&R) tools to make every attempt to meet the constraints, normally leading to unnecessary widening of logic blocks and duplication of logic and registers. It also discourages the tools from sharing logic resources. The same goal often can be achieved by specifying the maximum allowable timing slack, encouraging tools to optimize for smaller area and power.

What can be done to reduce power consumption at the board level?

For optimal power consumption, consider these factors:

- The device operating (junction) temperature: Reduce the junction temperature to reduce static power and increase device reliability and lifespan.
- Airflow: To reduce junction temperature, implement correct-by-design airflow. Allow for proper airflow around the FPGA by choosing low-profile regulators that won't cause thermal shadowing. This will allow for less expensive cooling solutions, such as smaller heatsinks, if any.
- Package spacing: Packages need to have proper spacing, with special consideration for keeping maximum distance between heat-producing parts.
- Package type: The choice of package can have a dramatic impact on power efficiency. If you can use a package like an LGA that solders directly to the PCB, the PCB then becomes the primary source of heat dissipation for that part.
- Efficient voltage conversion: To reduce power wasted in the power regulators, use converters with efficiency ratings of 90% and higher.

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