design FAQs

Clocking
Data Converters

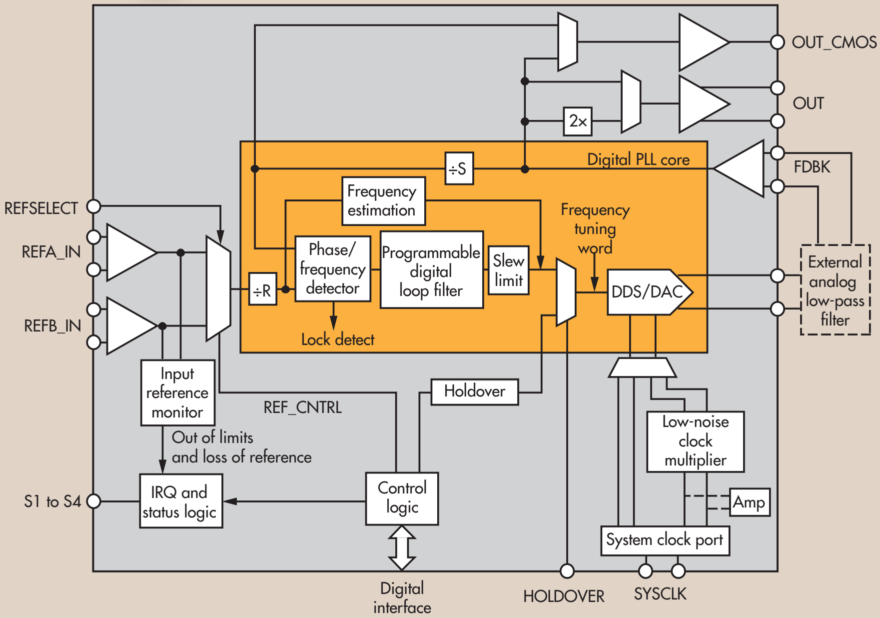
Don Tuite
Analog/Power Editor

What is the most critical performance characteristic for clock chips used with high-performance data converters?

The clock signal's phase noise (or jitter—the time-domain representation of phase noise) is the most critical spec. But also, pay attention to the band over which the jitter has been integrated. Phase noise limits signal-to-noise ratio (SNR).

For converter applications, broadband RMS additive jitter is a good specification to compare. For networking applications, specific offset bandwidths, such as 12 kHz to 20 MHz or 5 to 80 MHz, are typically specified. Either way, be sure to check the conditions for measurement. A faster slew rate, for example, will result in better SNR in data-converter applications. Additionally, measuring over a restricted band of offsets reduces jitter magnitude.

The highest-performance, high-speed converters require clocks with RMS jitter under 200 fs to achieve the highest SNR, so you should choose the lowest possible jitter under your conditions. If the number of outputs is not high enough, add fanout clock buffers of less than 100 fs to avoid inserting too much additive jitter into the clock chain.

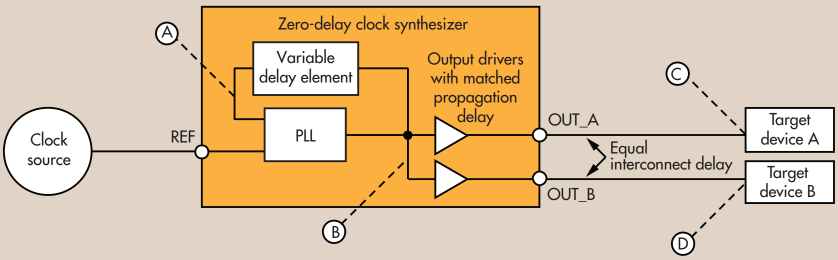


1. The output of the Analog Devices AD9549 digital-PLL clock device is directly related in phase and frequency to the selected reference. However, the system clock primarily governs its phase-noise spectrum. A programmable digital filter in the PLL core reduces any jitter on the reference.

What kinds of clock chips are available for driving data converters?

Clocking chips can be based on analog or digital phase-locked loops (PLLs). They may include integer and fractional-N PLLs, as well as devices with as many as four PLLs. Although there is no significant reason to prefer either analog or digital as the base technology for the PLL, there are concerns about fractional-N PLLs and multiple-PLL devices. Specifically, the spurs that result from implementing a fractional-N PLL are virtually always problematic.

A new breed of clock device that uses cascaded PLLs provides improved jitter performance. It uses a front-end loop with a very narrow loop filter to establish a very clean reference source to a second (back-end) PLL that enables chip designers to take relatively noisy system reference clocks and generate output signals with very low SNR *(Fig. 1)*.



2. An integrated zero-delay clock synthesizer comprises a PLL, two (or more) output drivers with matched propagation delay, and a variable delay element in the PLL feedback path. It also requires equal interconnect delay from the synthesizer outputs to their associated target devices. The PLL aligns the clock edges at Point A with the REF clock edges. The variable delay element in the PLL feedback path causes the clock edges at Point B to precede those at Point A by the amount of the variable delay. The variable delay is set equal to the sum of the output driver propagation delay and the interconnect delay, so the clock edges at Point C coincide with those at Point A, which coincide with the REF clock edges.

What logic levels are used for converter clock signals?

Most of today's converters use differential, low-voltage, positive emitter-coupled logic (LVPECL), based on a 3.3-V supply, with low and high thresholds of 1.6 and 2.4 V. Compared to low-voltage differential signaling (LVDS), LVPECL clock edges are faster, resulting in less time uncertainty for the converter's clock input buffer. Other logic levels, such as high-speed transition logic (HSTL), are sometimes seen. These provide still sharper edges and can enable even better SNR, as long as the signal can be terminated appropriately.

What's the best way to accommodate the need for multiple clock signals?

Many devices, such as FPGAs and complex programmable logic devices (CPLDs), don't need the same level of performance as data converters. They often can utilize the same (or an integer-related) frequency as the converters. The same base clock can easily support them as long as there is a sufficient number of outputs from the clock device.

As systems become more complex, the number of clock signals needed on a board keeps growing. But at the same time, there are good reasons (cross-talk, electromagnetic interference, and signal degradation, to name a few) to limit the number of clock traces routed across a circuit board.

Very low-jitter, high-toggle-rate, low-power LVPECL buffers can clock the additional converter channels to get the best SNR performance from the high-speed, high-resolution converters. (Very low-power, low-cost, highly integrated LVDS buffers are used for FPGAs.)

High-channel-density clock distribution products and high-fanout clock generators are available, but they can't always answer the full need, so simple but high-performing clock buffers or dividers and devices with narrow fanout are available.

What is "zero delay," and why do I need it?

Zero delay refers to a clock synthesizer's ability to provide an output signal that is edge aligned with a clock reference source (*Fig. 2*). Applications include many synchronous systems, such as the SONET and synchronous digital hierarchy (SDH) networks, high-speed network servers, and network line cards, as well as baseband timing for W-CDMA and Wi-Fi.