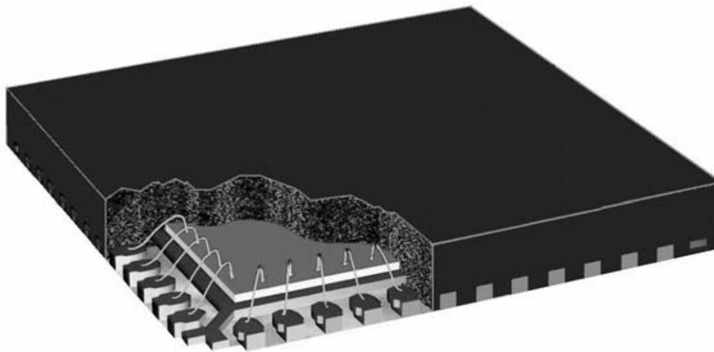
“Green” QFN Packages from Texas Instruments

Richard Saye

INTRODUCTION

Texas Instruments (TI) has recently taken proactive steps to introduce its package options as “Green,” including its Quad Flat No-lead (QFN) packages. The QFN packages are near-chip-scale plastic encapsulated packages that use conventional copper lead frame technology, without peripherally protruding leads, within their construction. Leads that are platted with NiPdAu to achieve a RoHS compatible Pb-Free finish that avoid problematic Sn (tin) platting known to produce whiskers. Also “Green” by utilizing mold compounds that exclude hazardous substances antimony and bromine that may soon join Pb (lead) as prohibited RoHS material. This assembly results in a cost-effective environmentally friendly packaging solution utilizing superior materials that allow a 260C reflow, maximize board space with added benefits of improved electrical and thermal performance over traditional leaded packages. QFN packages have an exposed pad that enhances the thermal and electrical characteristics, enabling high-power and high-frequency applications.



Illustrated Cut Out QFN Package

Sectional View Soldered QFN Lead

SOLDERABILITY TESTING

Normally solderability testing of finished integrated circuit (IC) packages is performed in order to predict performance of these devices in an actual printed circuit board reflow process. The "Dip-and-Look" (DNL) test method (TI’s QSS 009-130) is the electronics industry standard test method for solderability testing the leads of finished IC devices (ANSI/JSTD-002). This test method consists of immersing the IC leads into a rosin type flux for 5-10 seconds prior to immersion into molten 63% Sn/ 37% Pb solder for 5-10 seconds. Upon removal from the solder, the leads are cleaned and visually inspected using 10x optical inspection. The percentage of the lead surface not wetted by the solder is calculated. Industry standards specify that "all terminations shall exhibit a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination". Yet this ANSI/JSTD-002 solderability test is not as applicable in

today's Pb-free environment due to the lower temperature requirements of SnPb solder and non PWB attachment. The Surface Mount Solderability Test Method (SMT test) utilized within this report is intended to simulate the actual environment which surface mount devices encounter during the solder reflow process.

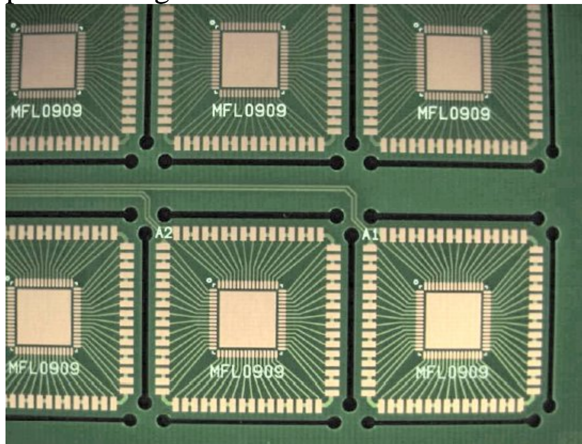
For this testing PWB and stencil were designed specifically for the QFN package. Refer to Application Note, Quad Flat-Pack No Lead Packages, Texas Instruments Literature No. SCBA017, SLUA271, Product Data Sheets for specific thermal information, via, and recommended PWB board layout. These documents are available at www.ti.com.

Although TI recommends NSMD (Non Solder Mask Defined) pads over SMD (Solder Mask Defined) pads when surface mounting QFN's both can be utilized. NSDM allows tighter tolerance on copper etching and by design provides a larger solderable area due to the exposed edges free from solder mask, thus providing improved solder-joint reliability. Additionally, SMD designs will inherently create stress points where the solder wets to the top of the pad on top of the lead. This stress concentration point is eliminated when the solder is allowed to contact the sides of the leads in NSMD designs.

There are several performance issues that need review when designing stencils.

- Control of the aperture size, including length with and thickness of stencil aperture's paste release characteristics as it is desirable that all paste is released to the PWB pads.
- Factures that can affect the paste release; are laser cutting with trapezoidal walls and rounding corners and preferably electropolished or electropolishing with nickel platting.
- Utilizing a print-area ratio (PAR) guideline to quantify the paste release capability of an aperture design. Acceptable results are normally archived when this PAR ratio is above 0.66, yet better release is accomplished when the ratio is above 0.75.
- Positional accuracy of the aperture location must be well controlled to avoid solder misregistration.

Customers should contact their board assembly site for recommended solder mask tolerances, via tenting, and stencil design recommendations. Refer to IPC 7525 for stencil design considerations and IPC-SM-782 as an alternate information source for PCB land pattern designs.



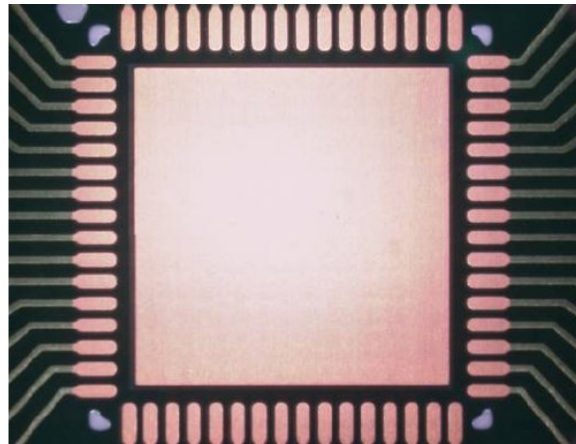


Figure 1: QFN Test Board designed per IPC standard.

Figure 2: QFN land pattern

QFN packages are soldered using SnAgAu paste and PWB mounted. TI recommends following the solder paste supplier's recommendations to optimize flux activity and also to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20.

TI also recommends the use of type 3 or finer solder paste when mounting QFN's. The use of paste offers the following advantages:

- Contains flux to aid wetting of the solder to the PCB land.
- The adhesive properties of the paste will hold the component in place during manufacture.
- Paste by volume contains around 50% metal load typically and can be varied by print volume for calculating the amount of paste necessary to form a given solder joint. QFN's are typically manufactured with printed center pad volumes between 50% and 80% by area to facilitate wetting of the periphery solder joints and also to maintain a standoff from the board surface.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

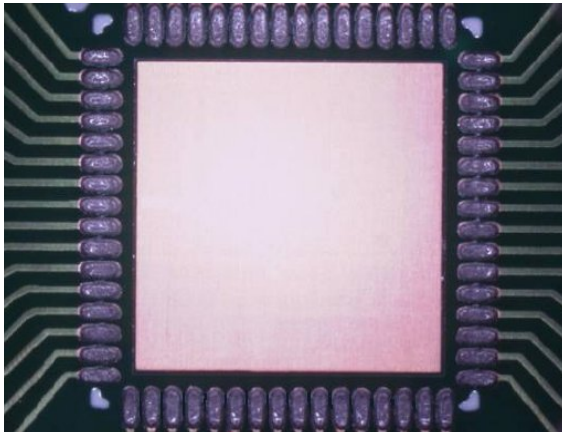


Figure 5; Solder Applied (center pad not soldered for this testing, normally minimum 50% coverage is recommended for the center pad)

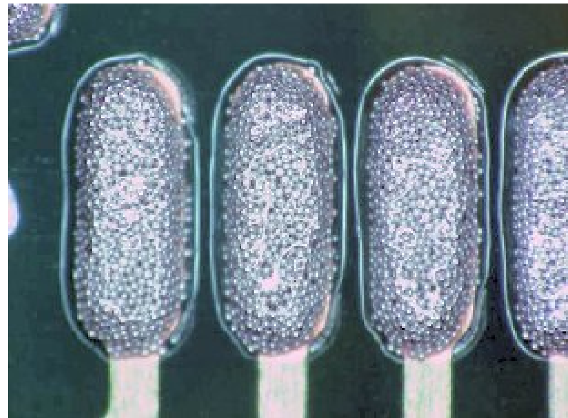


Figure 6; Close Up Soldered Leads

Note due to minimal package weight of TI QFN's reflow oven's air flow might need monitoring to insure package shift during reflow will not occur.

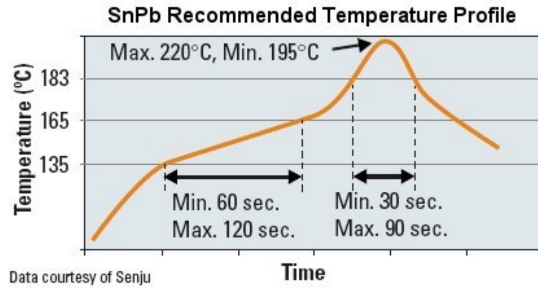


Figure 3; TI QFN's are compatible with SnPb Profiles (Shown only as reference)

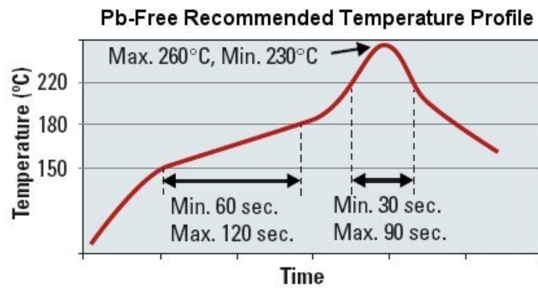


Figure 4; Pb-Free temperature profile used in testing

Figures above illustrates a range of temperatures that TI QFN packages are capable of withstanding without risk to package reliability but TI prefers parts to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. In general, the temperature of the part should be raised not more than 2°C/sec during the initial stages of the reflow profile. The exact profile would depend on the maximum peak temperature for the component as rated on the MSL label, the solder paste manufacturer's recommendation, complexity of the PWB, and capability of the reflow equipment to be confirmed by the SMT assembly operation.

The requirement to steam age QFN's within this test has been designated to simulate extended time periods between testing and soldering (>6 months) and have either limited thermal exposure or multiple thermal exposures before soldering. This current requirement assumes that "properly applied NiPdAu platting can withstand the steam conditioning environment well beyond the eight hours specified and may survive natural aging well beyond 12 months". Steam aging samples prior to testing may become more critical as the shelf-life of components and boards is reduced.

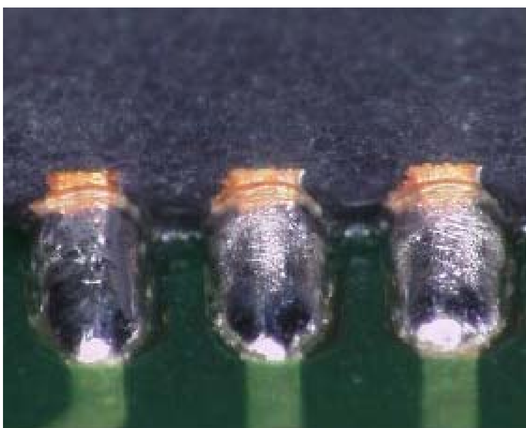


Figure 7; Solderability Testing Unit without Steam Ageing

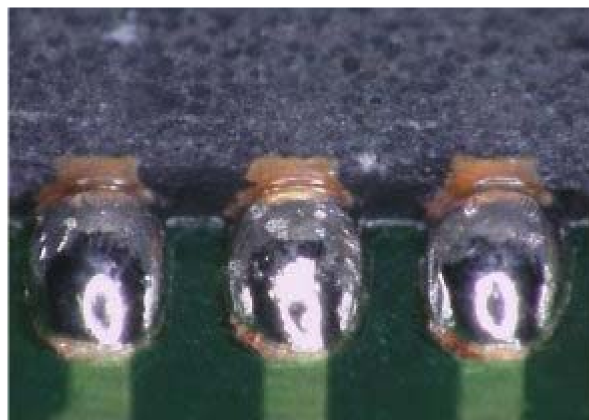


Figure 8; Solderability Testing Unit with 8 hour Steam Ageing

Results of solderability testing showed all units passed visual and X-ray inspection and electrical testing possible with utilization of a daisy chained die. The best possible

perimeter solder joints will have a good fillet on outside and a 50 – 75 micro standoff height. Additionally solder joints should have enough volume so an “Hour Glass” shaped connection is not formed. The electrical connection to the perimeter pads is made on the bottom of the package. Thus solder wetting and electrical connection to the sides of the QFN are not guarantied as the sides are not platted. For additional industry standards information on solder requirements see IPC/EIA J-Std-001C Section 9.2.6.4 and/or IPC A-610D.

Additionally, testing was done temperature cycling PWB mounted QFN’s at a range of -40°C to +125°C profile with a 10 minute ramp 10 minute dwell. Failure definition is the sample reaching 1.2x Initial Resistance. Both preconditioned (steam aged) and non-preconditioned devices were utilized within this testing. Package utilized was a 9 x 9 mm 64-RGC QFN that is defined “Green”. (Pb-Free no antimony nor bromine within it’s construction) Conclusion was all units passed thermo cycling with average group one failures occurring at 5704 and group two occurring 5155.

As part of TI internal qualification requirements drop testing was also completed on these QFN packages with test. Testing conditions were as follows; Board 8 layers, 1mm thick 101 x 48 x 1.120, Drop Conditions are 1500G with a one millisecond pulse, Failure definition is sample reaching 1.2x Initial Resistance. Conclusion was all units passed beyond the 40 drop requirement with average determined to be 233 drops.

In today’s manufacturing environment aggressively miniaturizing electronic produces driven primarily by the consumer markets need in reducing weight and height while still improving electrical performance and functionality Texas Instruments QFN packaging is the right fit. These packages meet forthcoming RoHS material restrictions requiring Pb-free devices and exceed material restrictions by removing elements antimony & bromine used as fire retardants. Additional information on Texas Instruments QFN’s are available at www.ti.com.